Supplementary Information to:

A Germanium Nanowire Reconfigurable Transistor Model for Predictive Technology Evaluation

By

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'14nm_node_GeRFET' Model Files:

The files '**14nm_node_GeRFET.zip'** available for download under: https://cfaed.tu-dresden.de/pd-downloads and comprises the necessary data to run predictive circuit simulations as described in the main manuscript. This supplementary document contains some helpful information regarding the use of the data files.

Major Compnent Descrition:

- Verilog A Syntax Files
- Three Versions of the data table with different exactness (full; halved; quarter)
- Circuit Design Symbol
- Layout Symbol

File Size:

The file size of the .zip is below 10 MB.

Platform/ Environment:

The files can be run on any circuit simulation tool, but we recommend Cadence Virtuoso. Two standard libraries needed to run the model are:

"constants.vams"

"disciplines.vams"

Setup/ Run Instructions:

The following steps describe an installation on Cadence Virtuoso. In another environment, this might differ.

1. Unpack the .zip files.
2. Copy the folder to the home folder or any subfolder on your circuit simulation facility
3. Add the line 'DEFINE GeRFET14nm /home/14nm_node_GeRFET to the cds.lib file of Cadence.
4. 'GeRFET14nm' should now be available in the library manager. If not, please check the library path editor and check if the data path is displayed correctly.
5. In the Library Manager 'RFET' should be visible in the cell view. The *symbol, layout,* and *veriloga* folders can be selected.
6. In the veriloga files, the following string selects the data table used:

   parameter string RFET_table = "RFETsmooth_Q.csv"

   It can be chosen between *RFETsmooth_Q.csv, RFETsmooth_Q_halved.csv,* and *RFETsmooth_Q_halved_02.csv*

7. The split matrix coefficients used can be adjusted manually in the Verilog-A code at ***real s_coeffs[0:35]=[…]*** As a standard, the matrix [S_{M1}] from the publication is used.
8. The RFET symbol can be used to generate and test circuit designs. Note that both program gates are coupled in this model version and cannot be steered independently.

Output description:

This model describes a general RFET for a device design with three gates having a dependent polarity control of both program gates aligned at source and drain. The model has 5 pins, S, PG1, CG, PG2, and D. Notice that V_PG1 and V_PG2 are always swept together; they are meant to be set at the same voltage. Therefore, pins PG1 and PG2 should always be short-circuited outside the symbol. If they are not, there is a variable V_PG defined to be the average of V_PG1 and VPG2. The nominal operating range of the RFET is +/- 0.8 V. In order to prevent to model from extrapolating, the table covers a range of up to +/- 1.3 V. A typical DC output of the model is given in Fig. 1.

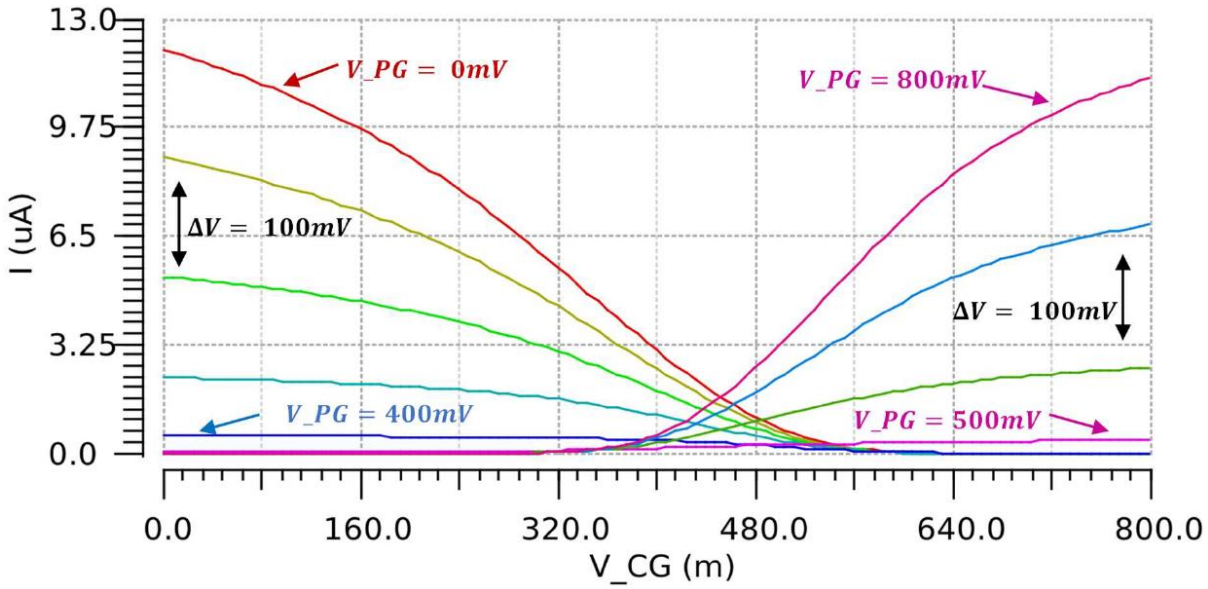

Figure 1: DC transfer characteristics (I_D-V_CG) of the 14nm_node_GeRFET table model for various values of V_PG. A supply voltage of V_DD= 800 mV is generally assumed.

Symbol and Layout Information:

Figure 2 shows the symbol used for the RFET. It is similar to standard MOSFETs but has three gates instead of one. The five pins are named after their abbreviations, which stand for S, PG1, CG, PG2, and D. A layout symbol is added for informational purposes. The exact dimensions have to be adjusted prior to use.

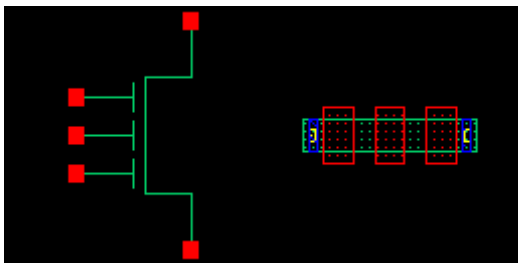

Figure 2: Symbol (left) and simple layout (right) provided with the Verilog-A table model data set.

Contact information:

For issues and requests regarding the model files, you can contact jens.trommer[at]namlab.com or akash.kumar[at]tu-dresden.de