Designing Efficient Circuits Based on Runtime-Reconfigurable Field-Effect Transistors

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***Abstract*— An early evaluation in terms of circuit design is essential in order to assess the feasibility and practicability aspects for emerging nanotechnologies. Reconfigurable nanotechnologies, such as silicon or germanium nanowire-based reconfigurable field-effect transistors, hold great promise as suitable primitives for enabling multiple functionalities per computational unit. However, contemporary CMOS circuit designs when applied directly with this emerging nanotechnology often result in suboptimal designs. For example, 31% and 71% larger area was obtained for our two exemplary designs. Hence, new approaches delivering tailored circuit designs are needed to truly tap the exciting feature set of these reconfigurable nanotechnologies. To this effect, we propose six functionally enhanced logic gates based on a reconfigurable nanowire technology and employ these logic gates in efficient circuit designs. We carry out a detailed comparative study for a reconfigurable multifunctional circuit, which shows better normalized circuit delay (20.14%), area (32.40%), and activity as the power metric (40%) while exhibiting similar functionality as compared with the CMOS reference design. We further propose a novel design for a 1-bit arithmetic logic unit-based on silicon nanowire reconfigurable FETs with the area, normalized circuit delay, and activity gains of 30%, 34%, and 36%, respectively, as compared with the contemporary CMOS version.**

***Index Terms*— Functionally enhanced logic gates, multi-independent gate reconfigurable field-effect transistor (MIGRFET), RFET, reconfigurable transistor, silicon nanowire (SiNW) transistor, three-independent gate field-effect transistor (TIGFET).**

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I. Introduction

APPLICATION-SPECIFIC integrated circuits (ASICs) based on CMOS technology have been the workhorse of electronic engineers as they boast of a circuit suited for a "specific" purpose with high performance to area ratio. This static design of CMOS technology is simple to build and is applicable to a wide range of application scenarios. These unique properties have been backed by technology downscaling of transistor sizes which leads to a lower cost per function [1]. With CMOS achieving dimensions below 28 nm, further scaling is still possible, but associated with a reduced cost and performance benefit [2], to support the growing demands of electronics industry.

Several emerging nanotechnologies, such as carbon nanotubes [3], [4], silicon nanowires (SiNW) [5]–[7], germanium nanowires [8], graphene nanoribons [9], and recently 2-D materials such as WSe_2 [10], [11], have been shown to exhibit the ambipolar conduction. Such reconfigurable technology can be exploited to achieve extended functionalities per unit area. The added functionality can be tapped to develop disruptive reconfigurable circuits with higher performance. For example, De Marchi *et al.* [7] showed that XOR operation is embedded in the characteristics of SiNW reconfigurable field-effect transistors (SiNW RFETs). In contrast to other nanotechnologies, such as the ones based on carbon nanotubes, graphene, or other 2-D materials, silicon and germanium nanowires support a mature top-down fabrication process [12], [13] and can readily use the existing technology infrastructure. Single-nanowire RFETs with full current–voltage (I–V) symmetry between p- and n-function have been shown experimentally by Heinzig *et al.* [5], [14]. The symmetry is a mandatory prerequisite to exploit runtime reconfigurability to enable the design of efficient and programmable logic gates as shown in [15]. Thus, it is already shown that SiNW RFETs exhibit higher logical functionality per unit area as compared with CMOS conventional switches. That is why the contemporary circuit designs when applied directly with RFETs cannot truly harness the benefits of newer nanotechnology. Circuit designs should precisely and efficiently employ the feature set of these new devices [16].

In this paper, we first discuss the device characteristics and functionality of SiNW-based reconfigurable transistors with

dual and multiple independent gates and elaborate on how they can be used as a promising new reconfigurable technology. We further demonstrate how transistor-level dynamic reconfigurability can be used to achieve functionally enhanced logic gates. We propose six such functionally enhanced logic gates that can enable a reconfigurable circuit design. With the help of comparative analysis for exemplary CMOS-based circuits, we show how an RFET solution exploiting device-level reconfiguration renders equal functionality as CMOS with fewer resources. Furthermore, to show the potential of our approach, we present a novel design for a 1-bit arithmetic logic unit (ALU) using device-level reconfigurability. While the focus of this paper is SiNW-based reconfigurable FETs, the concepts shown here are applicable to other reconfigurable technologies as well.

Major contributions of this paper to improve the state of the art are in the following.

1) A list of functionally enhanced logic gates along with their detailed evaluation has been proposed to facilitate the design flow using reconfigurable nanowire technology.
2) Demonstration of runtime reconfigurability [17] on the example of the multifunctional circuit and its ability to replace common multilevel MUX-trees. This helps to explore the design space between higher functional expression and performance.
3) Comparison of multifunctional circuit implemented in the standard CMOS and reconfigurable nanowire technology with the result of up to 32% normalized delay, 20% area, and 40% power consumption (in terms of activity) improvements by using RFETs over the standard CMOS.
4) A novel 1-bit ALU design is implemented with RFETs and, in comparison to existing CMOS implementations, has been shown in terms of the normalized circuit delay, area, and activity.

The remainder of this paper is organized as follows. Section II gives details about the motivation of the work presented in this paper and lays the basic background. Section III enumerates the functionally enhanced logic gates made of reconfigurable FETs, compares them with CMOS technology, and explains the technology-independent logical effort calculation and the dynamic reconfigurable operation with reconfigurable transistors. Section IV introduces a multifunctional circuit and is followed by a novel ALU circuit design in Section V. Conclusions and proposals for future work are given in Section VI.

II. Background and Motivation

A reconfigurable (also called polarity-controllable) device is a functional element, which can dynamically switch between p-type conduction and n-type conduction by means of an electrical programing signal. These devices offer hardware flexibility from the technology itself. Such devices have been shown using a wide range of materials ranging from silicon [5], germanium [18] to carbon nanotubes [3] and recently 2-D materials, such as WSe_2 [19].

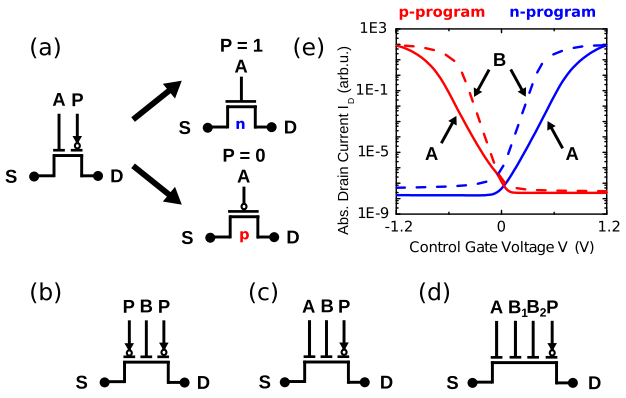

Fig. 1. Schematic circuit symbols and exemplary transfer characteristics of various reconfigurable nanowire transistor types. (a) Dual-gate RFET, which can represent n-MOSFET or p-MOSFET characteristics (input A) depending on the programing signal P. Extended reconfigurable design options, such as (b) three-gate RFET with CG (input B) in the middle of the channel, (c) TIGRFET combining inputs A and B, and (d) MIGFETs with a total of four gates. (e) Simulated I–V transfer characteristics achieved with the logical inputs A and B for p-type (red curve) and n-type (blue curve) configuration of the transistor shown in (c). The I–V characteristics of the transistor types in (b)–(d) have a similar shape.

Most of the research studies, however, have focused on SiNW-based devices. Here, the bimodal-conduction functionality is enabled by longitudinal metal-$NiSi_2$/intrinsic-Si/metal-$NiSi_2$ nanowire heterostructures forming Schottky junctions with the silicon, which are controlled by two or more independent gates. The materials and processes applied for the fabrication are fully CMOS compatible. Thus, various types of such SiNW Schottky barrier transistors, that enable the runtime reconfiguration between the p- and n-functions, have been demonstrated within recent years [6], [7], [14], [20], [21]. An introductory review on their functionality can be found in [22]. A more in-depth description of the device physics of these transistors can be found in [23].

In this paper, we focus on the resulting reconfigurable functionality out of these devices instead. The schematic of a simple realization with two individual top gates, as built by Heinzig *et al.* [5], is shown in Fig. 1(a). In this dual-gate approach, the gate overlapping the source junction is named control gate (CG) as it controls the carrier flow, just like in the standard CMOS device. The additional gate aligned on top of the drain contact is used to program the transistor by blocking the undesired carrier type and, thus is called program gate (PG). Depending on the voltage scheme, the device exhibits either p-type functionality (P = "0," red line) as shown in Fig. 1(e), meaning the current output is high when the input voltage at A is low, or n-type functionality (P = "1," blue line), meaning the current output is high when the applied control potential (A) is high.

A mandatory requirement for the practical use of reconfigurable transistors is that both program types have to deliver the same output current at an identical geometry. This has been experimentally demonstrated for the first time by Heinzig *et al.* [14], therefore enabling truly complementary inverter circuits using a single supply voltage. This fully symmetrical I–V characteristics can be seen in

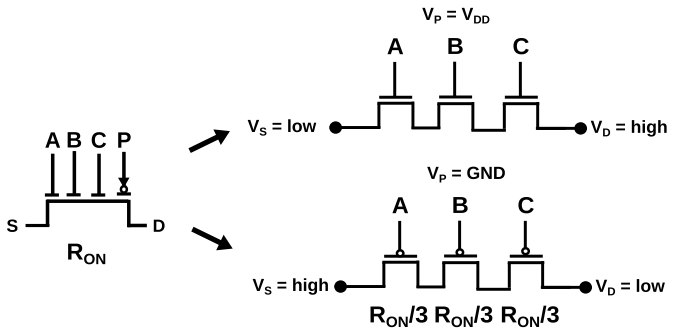

Fig. 2. Equivalent circuit of a multigate RFET with four gates. One single transistor resembles three single-gated transistors in series. All three transistors are programed to p- or n-functionality depending on the applied voltage scheme. In addition, they virtually operate with an effective resistance of only (1/3) of the internal resistance of the device.

Fig. 1(e) as determined here from technology computer-aided design simulations (symmetry of curves along the axis CG voltage = 0 V).

Another prominent feature of the RFET is that the device is operable even with an ungated area in the middle of the channel. This gives rise to the opportunity of adding additional independent gates to the channel. Although this will slightly increase the channel resistance, the effect is much smaller than in the classical CMOS technology, owing to the presence of a Schottky barrier in the ON-state of a RFET [15]. If the transistor is controlled by the potential applied at this channel gate (B), as shown in Fig. 1(b), lower threshold voltages and steeper subthreshold slopes can be achieved. Both modes (A and B) can be observed from a single transistor [see Fig. 1(c)]. This concept has been experimentally proven by Zhang *et al.* [6] showing devices containing three independent gates and was extended to larger multigate RFETs by Trommer *et al*. [15] as shown in Fig. 1(d). The associated device characteristics accessed by finite element simulations are shown in Fig. 1(e).

These multigate transistors, therefore, only pass a current if all CGs are in the ON-state at the same time. Consequently, each MIGRFET can be described by an equivalent circuit consisting of several standard FETs in series as shown in Fig. 2. This equals a wired-AND functionality enabled by a single device [13]. The PGs are used to set the polarity of the whole path (see Fig. 2). Remarkably, the ON-current for an individual multi-independent gate (MIG) device is equal regardless of whether if the transistor is steered directly at the source gate [Fig. 1(e), CG A, straight lines] or at the channel gate [Fig. 1(e), CG B, dashed lines]. This is reasoned in the fact that the ON-resistance of the device is limited by the injecting Schottky barrier as proven through measurements [5] and scanning gate microscopy analysis [24]. As a result, each of the inputs of a MIGRFET operates with a lower virtual channel resistance of only R_{ON}/m, where m is the number of input gates. Utilizing this effect, efficient combinational logic gates have been demonstrated in [15].

In addition, Zhang *et al*. [6] have shown that the input A can be treated as a low leakage mode, while the input B exhibits a higher transient performance due to their difference in threshold voltage and subthreshold slope [25]. This effect has to be taken into account by the circuit design. Preferably, no slow input (A) has to be placed on the critical path of a larger circuit design. In all of our exemplary circuit analysis, this condition is satisfied.

The above works lay the basic foundations for the need to formalize the process in order to tap the reconfigurability offered by these newer nanotechnologies. An important aspect is to use this device-level programmability at the circuit level to realize a runtime-reconfigurable circuit offering multiple functionalities. Marchi *et al.* [7] have shown that XOR functionality is embedded naturally within dually gated reconfigurable devices. Efficient arithmetic logic gates [26]–[29] and circuits [30]–[33] were demonstrated. Raitza *et al.* [34] and Gaillardon *et al.* [35] showed good savings in area and delay for larger circuits and ASICs, respectively. Recently, majority functionality is proposed as the natural abstraction for newer nanotechnologies [36]–[39]. Quantitative analysis in terms of parameter numbers clearly reveals that conventional circuit designs are suboptimal for newer nanotechnology and newer designs are essential for their true evaluation.

III. Efficient Combinational Logic Gates Based on Runtime-Reconfigurable FETs

Interesting logic gates using these RFETs can be realized. In this section, we first list these functional logic gates that can exhibit runtime-reconfigurability followed by an evaluation of their normalized gate delay using the logical effort theory and then discuss how runtime reconfiguration is possible.

A. Functionally Enhanced Logic Gates

The key combinations of logic gates have been enumerated in the following.

1) 2-NAND-NOR: Fig. 3(a) shows a MIN logic gate which can be reconfigured to NAND and NOR functionality. The value of P determines the final functionality of the MIN logic gate. As shown in the figure, the PG input of 0 delivers NAND and 1 gives NOR functionality. If a third input is connected to P, the functionality is boosted as the logic gate behaves as a MIN gate. The technical implementation is referred to as the pass transistor logic [17] since an inverter or network passes the rail voltages to the functional cell. The Boolean function can be represented as
$$f = (A * B + B * P + P * A)'. \tag{1}$$
2) 2-AND-OR: A trivial extension of the 2-NAND-2NOR gate is achieved by adding an output inverter. The resulting 2-AND-2OR Boolean function is represented as
$$f = (A * B + B * P + P * A). \tag{2}$$
3) 3-NAND-NOR: Fig. 3(b) shows a 3-NAND-NOR logic gate. The structure shows three dual-gate RFET connected in parallel with one MIG (four gate terminals) RFET connected at the bottom. SiNW-based RFETs offer to place multiple gates on a single wire without

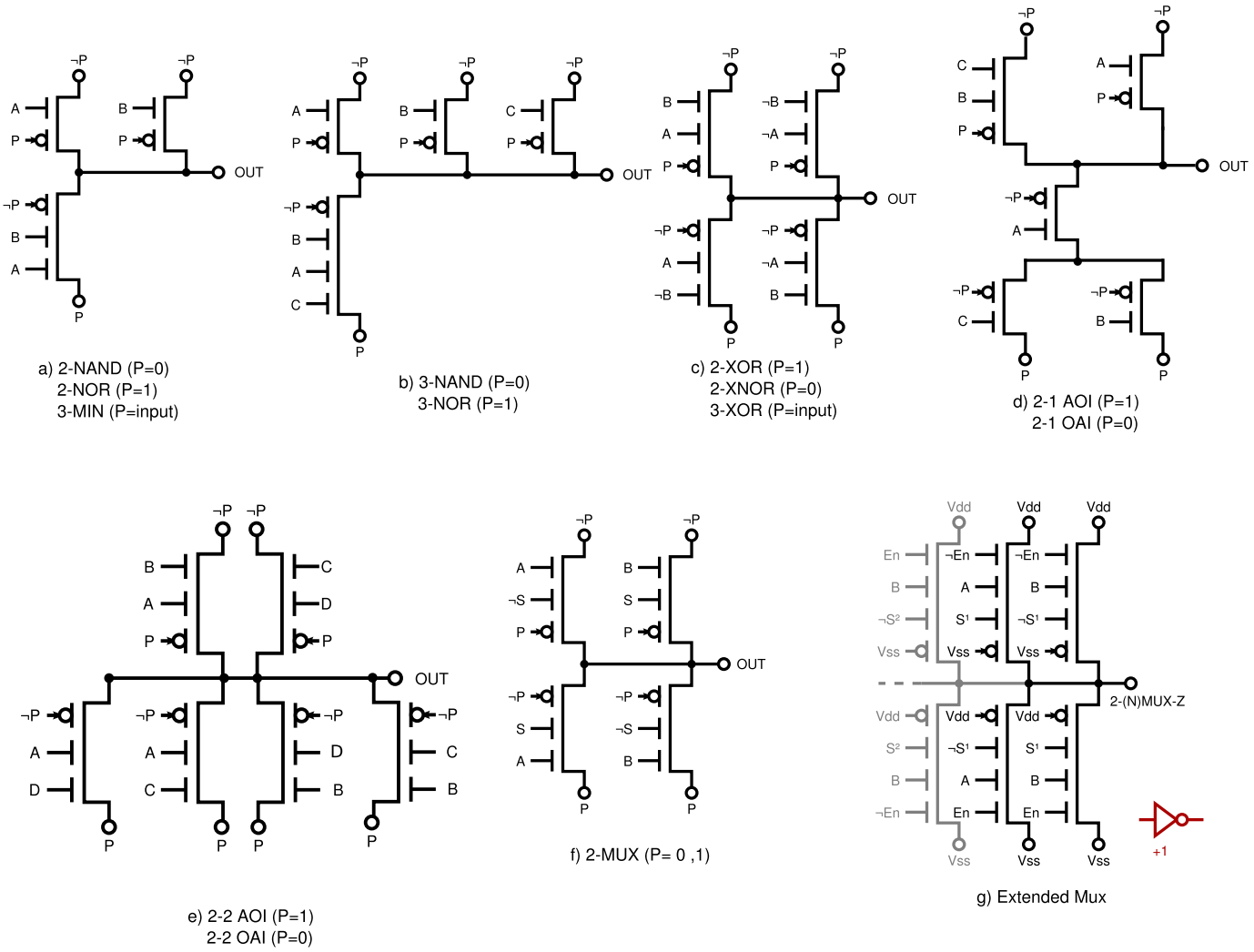

Fig. 3. Efficient combinational logic gates built from MIGRFET technology. (a) 2NAND and 2NOR. (b) 3NAND and 3NOR. (c) 2XOR and 2XNOR. (d) 2-to-1 AOI and OAI. (e) 2-to-2 AOI and OAI. (f) Inverting two-way MUX. (g) Extended MUX functionality. In the static case, the program signal P is set to GND (0) or V_{DD} (1). A dynamic switching between both functions can be achieved by altering the program signal. In addition, the gates in (a) and (c) can be executed in a transmission gate style by applying the PG as additional input signal to map the 3MIN and 3XOR function, respectively.

penalty in performance [34]. The Boolean function is represented as

$$f = (A + B + C) * P' + (A * B * C) * P. \quad (3)$$

4) 2-XOR-XNOR: Fig. 3(c) represents the 3-XOR logic gate functionality. The potential at P determines the actual function of the logic gate. If P is fed with the third input, then, the logic gate function will change from a 2-XOR/2-XNOR to a 3-XOR gate. The Boolean function is represented as

$$f = (A * B + A' * B') * P + (A * B' + A' * B) * P'. \quad (4)$$

5) 2-1 AOI-OAI: Fig. 3(d) represents an AOI-OAI21 logic gate. This logic gate was first demonstrated in [17], but the representation was only based on dual-gate RFETs. Here, we have used a combination of three-independent gate field-effect transistors and dual-gate RFETs to provide additional area savings. The Boolean function is represented as

$$f = (A * B + C)' * P + ((A + B) * C)' * P'. \quad (5)$$

6) 2-2 AOI-OAI: Fig. 3(e) represents the *AOI-OAI22* logic gate. The logic gate is similar to the *AOI-OAI21* version. The Boolean function is represented as

$$f = (A * B + C * D)' * P + ((A + B) * (C + D))' * P'. \quad (6)$$

B. Additional Logic Gates

While the above six logic gates support runtime reconfigurability, the following two logic gates are more efficient in terms of their performance and use MIG terminals to encapsulate more logic as compared with their CMOS counterparts.

1) MUX: Fig. 3(f) represents the inverting two-way MUX. MUX is used only in the static mode. The Boolean function is represented as

$$f = (A * S' + B * S) * P + (A * S + B * S')P'. \quad (7)$$

2) Extended MUX: Fig. 3(g) represents the extended multiplexer as used in [34]. Raitza *et al.* [34] used this *extended* MUX as a replacement for a two-stage multiplexer, and it can be seen as an important addition to the work. Such logic gates also demonstrate the fact that with SiNW RFETs, one can design more efficient and compact logic gate blocks. The Boolean function is represented as

$$f = (A * S_1' + B * (S_1 + S_2')) * En + (A * S_1 + B * (S_1' + S_2)) * En. \quad (8)$$

From the above list, we can see that all logical functions, which are available in CMOS-like generic library, can be efficiently implemented using reconfigurable FETs.

C. Estimation of Gate Delay Using the Logical Effort Theory

In order to make use of the above list of logic gates, it is important to find a measure for the performance of the above gates. Here, we analyze the delay of the proposed circuits using the logical effort theory [40] as described in [17]. The big advantage of this method is that it delivers technology-independent results, which are directly transferable from a micrometer-sized lab technology to highly integrated circuits. By reformulation of a simple RC-based model, the propagation delay t_{PD} through an arbitrary logic gate can be described as

$$t_{\mathrm{PD}} = \tau * D \quad (9)$$

with

$$D = gh + p \quad (10)$$

where τ is the intrinsic inverter delay, D is the structural delay of the circuit, h is the fan-out, p is called parasitic delay, and g is called logical effort, which is a direct measure for the logic inputs topological complexity. A higher logical effort is thereby associated with a higher amount of input capacitances, which have to be charged, and, thus, a larger circuit delay till the logic gate has successfully performed the output calculation.

However, for an overall delay comparison, the intrinsic inverter delay τ, which is a measure for the performance of the integrated technology, also has to be accounted for. In a first-order approximation, the intrinsic delay is inversely proportional to the ON-currents I_{on} of the individual device

$$\tau = V_{\mathrm{DD}} * C_G / I_{ON} \quad (11)$$

where V_{DD} is the supply voltage and C_G the input capacitance of a single input gate.

With fabricated demonstrator devices still lacking in terms of ON-current, the performance calculations done here can be easily transferred to a future highly scaled integrated technology. Recent simulation studies have shown that the scaling of device dimensions, and applying several stacked nanowires on the top of each other [10], [41] will increase the device performance of SiNW RFETs significantly. Moreover, promising performance projections are given for both germanium nanowires and carbon nanotubes [4], [18], [42]–[44], making it conceivable that similar delay values as state-of-the-art low-operation-power CMOS technology can be achieved. Noted that the real intrinsic delay value of an RFET technology is somewhere in the middle of an inverter circuit utilizing only low-leakage-type Schottky gates or high-performance channel gates (see Fig. 1). This is especially important within the critical path of a circuit, where only fast inputs should be used. However, utilizing the multigate technology, one can always add more gates to the channel and trade area for a better transient performance.

We treated τ as a technology-agnostic value for all analysis in this paper under the assumption that an intrinsic delay similar to that of a respective CMOS device can be achieved by implementing the above-described measures. Under this assumption, the logical effort and normalized delay can be used as a direct measure to compare the performance of a certain circuit layout. In the first analysis step, we assume that the logic gates shown in Fig. 3 are operated in a static mode. This means that all instances of P are directly connected to GND and all instances of $\overline{P}$ are directly connected to the supply voltage delivering a fixed functionality. In this configuration, the logic gates match their CMOS counterparts in terms of functionality.

Calculated values of g and p for the respective logic gates shown are given in Table I. It is evident that due to their lower transistor count, all proposed MIGRFET gates exhibit a reduced logical effort and less parasitic delay as compared to their CMOS counterparts. This performance increase is a result of the virtually lower channel resistance per input. In addition, there is always only a single transistor placed between the output node and the supply potentials, which omits the need for having several nanowires in parallel to speed up the serial branches. As a consequence, several changes in the circuit topology become evident here. First of all, NAND and NOR circuits can be built with equal performance, simplifying timing constraints. Second, for individual inputs, all sorts of NAND, NOR, and MUX gates have a logical effort value which is *equal* to that of an inverter. This connotes that they all have equal driving strength. As a result, multigate RFETs provide an increased design flexibility as all of those gates can be used to buffer a subsequent transmission gate, without an additional delay penalty. Moreover, it is evident that, especially, functions with a high number of inputs, such as AOI or EMUX, perform much better when built using an RFET technology.

D. Runtime Reconfiguration

If the proposed logic gates are applied for actual runtime-reconfiguration, the program signals P and $\overline{P}$ have to be switched dynamically. In the most simple implementation, this can be executed by a single inverter routing the program signals [45]. For the sake of delay analysis, the whole gate including this input inverter can be described as a new form of a transmission gate. The logical effort for this type of gates is calculated using the methodology introduced by Trommer *et al.* [17]. The resulting logical effort and delay values are given in Table II. It is obvious that the program

TABLE I

COMPARISON OF TRANSISTOR COUNT #T, TOTAL LOGICAL EFFORT gTOT, LOGICAL EFFORT PER INPUT SIGNAL gS, AND PARASITIC DELAY *p* FOR STATIC LOGIC IMPLEMENTATIONS OF THE GATES SHOWN IN FIG. 3

Gate	Variable	CMOS	MIGFET
Inverter	#T	2	2
	gTot	1	1
	gIN	1	1
	p	1	1
2-NAND	#T	4	3
	gTot	8/3	2
	gA/B	4/3	1
	p	2	3/2
2-NOR	#T	4	3
	gTot	10/3	2
	gA/B	5/3	1
	p	2	3/2
2-X(N)OR	#T	8	4
	gTot	8	4
	gA*/B*	4	2
	p	4	2
3-NAND	#T	6	4
	gTot	5	3
	gA/B/C	5/3	1
	p	3	2
3-NOR	#T	6	4
	gTot	7	3
	gA/B/C	7/3	1
	p	3	2
2-1AOI	#T	6	5
	gTot	17/3	9/2
	gA	5/3	3/2
	gB,C	2	3/2
	p	10/3	2
2-1OAI	#T	6	5
	gTot	16/3	9/2
	gA	4/3	3/2
	gB,C	2	3/2
	p	3	2
2-2 AOI	#T	8	6
	gTot	24	6
	gA,B,C,D	6	3/2
	p	6	2
2-MUX	#T	10	4
	gTot	8	4
	gA*,B*,C*	2	1
	p	4	2
2-EMUX	#T		6
	gTot		6
	gA*,B*,S*,En	N/A	1
	gS*,En		2
	p		2

TABLE II

COMPARISON OF TRANSISTOR COUNT #T, TOTAL LOGICAL EFFORT gTOT, LOGICAL EFFORT PER INPUT SIGNAL gS, AND PARASITIC DELAY *p* FOR THE SIX FUNCTIONALLY ENHANCED LOGIC GATES SHOWN IN FIG. 3

Gate	Variable	MIGFET
2-NAND/2-NOR RESPECTIVE 3MIN TRANSMISSION	#T	5
	gTot	11
	gA/B	2
	gp	7
	p	3
2-AND/OR (Fig. 3(a) + inv)	#T	7
	gTot	11
	gA/B	2
	gp	7
	p	4
2-XOR / 2-XNOR RESPECTIVE 3-XOR TRANSMISSION	#T	6
	gTot	16
	gA*/B*	4
	gp	8
	p	4
2-1AOI / 2-1 OAI	#T	7
	gTot	21
	gA/B/C	3
	gp	12
	p	4
2-2 AOI / 2-2 OAI	#T	8
	gTot	22
	gA/B/C/D	3
	gp	10
	p	6
3-NAND / 3-NOR	#T	6
	gTot	14
	gA/B/C	2
	gp	8
	p	4

signal comprises the largest logical effort (gP is much larger than gA/B/C) among all input signals. This simply means that the process of reconfiguration takes more time than the actual processing of the input signals A and B. Furthermore, as a tradeoff for the increased functionality, the logical effort values for the signals A and B double as compared with the static logic gate implementation, due to the fact that there is an additional transistor placed between the supply potential and the output node.

Interestingly, some of the proposed gates enable additional functions when used as the *pass transistor logic* [17], which means that a logic input is applied at the outer source and drain contacts of the logic gate. As a result, for example, the 2NAND/2NOR or the 2XOR/XNOR gate inherently supports the 3MIN and 3XOR function, respectively, if P is used as the third logical input signal. However, it can be noted that reconfigurability is available at the cost of an increased number of transistors and logical effort. This is because of the slow reconfiguration paths, comprising of large capacitances which have to be addressed during operation. Thus, it is important to have a closer look at individual circuit designs to exploit this added functionality. In Section IV, a simple, yet

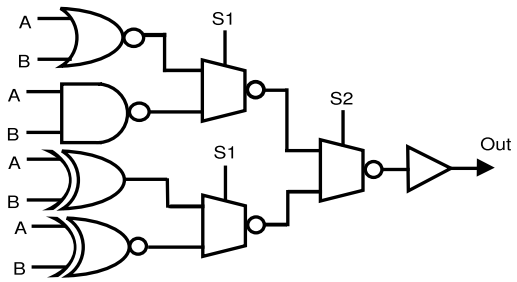

Fig. 4. Circuit with multiple functionalities based on CMOS.

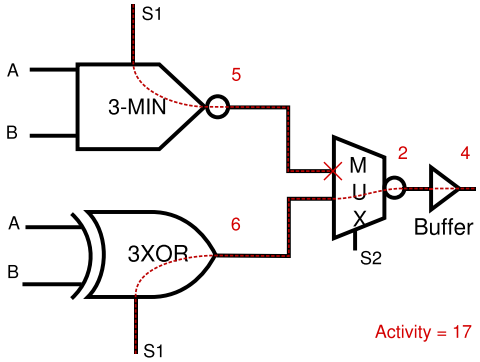

Fig. 5. Circuit with the pass transistor logic based on RFETs. The red lines show the path for maximum activity. The numbers show the maximum number of transistors affected, which are used for activity calculations.

powerful user-addressable multifunctional circuit cell based on reconfigurable technology is introduced.

IV. Multifunctional Circuit

The concept of transistor-level reconfigurability was introduced in previous works [11], [15], [34] but was restricted only to configurations, where a single logic gate can show multiple functionalities. In this paper, we start with a similar configuration of logic gates in a circuit as shown in [15]. In this paper, we consider logic gates in different configurations, such as static-logic and pass transistor logic, in order to have multiple analysis points.

For this paper, we consider the following assumptions.

1) For the logic gates, both normal and complemented inputs are available.
2) Since SiNW RFETs are still a lab technology, all numbers are normalized to the inverter of the respective technology for comparative reasons.
3) The circuits are designed in a way that no slow input (A) is placed on the critical path.

A. CMOS-Based Circuit Offering Multiple Runtime-Reconfigurable Functions

The CMOS technology exhibits fixed behavior per transistor. This fixed nature extends into logic gates primarily meant for a unique function. In order to realize runtime-reconfigurability, MUX-trees have been one of the most efficient solutions. Two logic gates, whose outputs are connected with a MUX, allow the user to choose between them at runtime using the select lines. So, in case of an exemplary CMOS-based circuit, for achieving functional reconfigurability among four logic functions from two inputs, a circuit as shown in Fig. 4 is required. The figure shows logic gates connected using a MUX-tree. The select lines S1 and S2 determine the functional output. The overall circuit consists of logic gates in the static mode. This is our reference circuit in CMOS technology.

B. RFET-Based Circuit in Pass Transistor Logic Offering Multiple Runtime-Reconfigurable Functions

The corresponding circuit to Fig. 4 as realized with functionally enhanced logic gates designed with reconfigurable transistors is shown in Fig. 5. It encompasses the following logic gates: 3-bit MIN, 3-bit XOR, and MUX. This circuit can be configured to deliver a range of logic functions. We first explain the logic gates based on RFETs used in this circuit along with the range of functions that can be computed. An inverter can be used to have the complemented functionality depending upon user's need.

1) Min Logic Gate: The top logic gate in the circuit of Fig. 5 shows a MIN gate [see Fig. 3(a)] having three inputs. The two inputs A and B are fed to the CG of the transistors, and the remaining input (S1, here) is fed to the PG. The three logic functions of NAND, NOR, and MIN are possible when S1 is a variable input (*reconfigurable layout* [46]) of the logic gate. Making S1 as a reconfigurable input leads to a delay penalty, but the positive tradeoff is the higher functional range.

2) Three-bit XOR Logic Gate: The second gate in Fig. 5 shows a 3-bit XOR logic gate [see Fig. 3(c)] in which similar to the previous logic gate, the two inputs A and B are fed to the CGs of the XOR gate while the third input, S1 is fed to the PG. If the logic gate is used in the pass transistor mode with 3-bit XOR functionality, then, S1 can be used to switch between 2-bit XOR and 2-bit XNOR logic functions. Similar to the Min logic gate, making S1 as the reconfigurable input degrades the performance of the logic gate but increases its functional range.

We have calculated the design parameters considering this configuration. This circuit is referred as RFET_Reconf in Table III.

C. Functional Analysis

In order to support the claim of efficient circuit designs with newer nanotechnologies, we evaluate the circuit shown in Fig. 5 with the MUX-tree-based circuit (see Fig. 4) in both CMOS and RFET technology. The MUX by itself is used for dynamic reconfigurability and has been an important building block for reconfigurable platform such as FPGA [47], [48]. That is primarily the reason for using MUX-tree for the CMOS circuit for runtime reconfigurability. To achieve similar functionality as the reconfigurable mode of the RFET circuit in CMOS technology, one needs a higher number of logic gates and a larger MUX tree. In contrast to the circuit shown in Fig. 5, a higher range of functions is observed with

TABLE III
COMPARISON IN TERMS OF NUMBER OF TRANSISTORS, AREA, NORMALIZED DELAY, AND ACTIVITY FOR CIRCUITS SHOWN IN FIGS. 4 AND 5

Circuit	No. of transistors	Area (μm^2)	Area gain w.r.t. CMOS (%)	Total normalized delay	Delay gain w.r.t. CMOS (%)	Activity	Activity gain over CMOS (%)
RFET_reconf (Fig. 5)	25	4.23	20.14	19.13	32.40	17	40
RFET_MUX_ckt (Fig. 4)	38	6.93	-30.69	18.8	33.57	26	7
CMOS Circuit (Fig. 4)	88	5.30	Reference	28.3	Reference	28	Reference

TABLE IV
VARIABILITY OF FUNCTIONS UPON CHANGING VALUES OF S1 AND S2 FOR MULTIFUNCTIONAL CIRCUIT SHOWN IN FIG. 5

S2	S1	Functionality Realized
0	0	2-bit XNOR
0	1	2-bit XOR
0	Input	3-bit XOR
1	0	2-bit NAND
1	1	2-bit NOR
1	Input	Minority

runtime reconfigurability offered from the technology itself. Individually, each logic gate based on RFETs delivers more than one functions. The ensemble of each variety of such combinations leads to many unique logical functions.

Table IV shows the complete list of logical functions that are possible using the circuit in Fig. 5 with all the variations of S1 and S2. The value of S2 for the MUX is used to select between the MIN and 3-bit XOR functionality.

D. Circuit Analysis of the Network

In this section, we evaluate the circuits in terms of area, delay, and activity. For delay calculation, we have used the logical effort theory. For area estimation, we have used multiplication factor with an inverter area in their respective technologies. Table III shows the calculation done for various circuits. We have used three circuits for our study: the RFET_Reconf logic circuit, the RFET-based MUX-tree circuit, and, finally, the CMOS-based MUX-tree circuit, which is the baseline reference for our calculation.

1) Number of Transistors: For the number of transistors calculation as shown in Table III, RFET-based circuits have a lower number of transistors as compared with the CMOS-based circuit because of their higher functional expression. In terms of the number of transistors, the RFET-based circuit has 50%–80% reduction as compared with the CMOS baseline. Having said that, an individual RFET is larger as compared with the CMOS transistor, a detailed analysis in terms of area has been shown below.

2) Area: For actual area (in μm^2) comparison, we use the open source library for CMOS at the 45-nm technology from *FreePDK45* [49] and the 22-nm SOI-based SiNW RFET library [50] with technology scaling [51]. Furthermore, we use the area numbers for inverters in both technologies to get an estimate of the postphysical synthesis area for the above circuits as shown in [50] as all the logic gates are not available for RFETs. The area of inverter in RFET and CMOS technologies (scaled to 22 nm) is 0.296 and 0.12 μm^2, respectively. It is important to note that the area mentioned in [50] was for logic gates consisting only of *dual-gate RFETs*. In order to yield realistic area calculations, we use the multiplication factors of 7/5 and 9/5 for three independent gate (TIG) RFETs [15] and four-gated MIGRFETs [15] with respect to the simple dual-gate RFETs. The numbers are consistent with the finite-element models used to simulate the characteristics shown in Fig. 1.

Despite of the fact that the individual transistor in RFET technology is almost two times the size of the CMOS transistors, the area of the RFET-based circuit is smaller as compared with that of the CMOS-based circuit. The RFET_reconf logic circuit in Fig. 5 is the smallest circuit with an area 20% smaller than that of the CMOS reference circuit. In terms of area, the MUX-tree implementation in RFET technology is the least efficient of all and is 31% larger than the CMOS reference circuit.

3) Delay: The nominal circuit delay of the multifunctional circuits, shown in Figs. 4 and 5, has been estimated using the method of logical effort. Thereto, the approximate minimal delay of each individual path through the circuits is calculated using the following expression:

$$D_{\min} = \left(h \prod g_i b_i\right)^{\frac{1}{N}} + \sum p_i \tag{12}$$

where N is the number of stages within the path, g_i and p_i are the logical effort and parasitic delay values of the individual stages, respectively, h is the fan-out of the whole path, and b_i is the branching effort of every stage. Each input is, therefore, considered to be fed by an inverter. A general fan-out of 4 is used for calculation. The delay of the slowest individual path, the so-called critical path, is then considered the nominal delay of the whole circuit. As stated earlier, all results are under the assumption, that a similar individual device performance of RFETs and CMOS devices can be achieved, e.g., with the use of germanium nanowire channels or 2-D materials such as WSe_2.

Given this assumption, it can be seen in Table III that a high gain of 34% in nominal delay is achieved if the standard MUX-tree circuit (see Fig. 4) is built with RFET devices. This is reasoned in the fact that the inverted MUX logic gate [see Fig. 3(e)] performs significantly better in RFET technology, as it is completely static. However, as discussed in the area section, this layout would come with an extreme area overhead. Therefore, the proposed novel multifunctional circuit is needed. For the RFET_reconf logic circuit, the delay is 33% lower as compared with the CMOS circuit delay, as the

involved gates used for reconfiguration are more efficient (3-MIN and 3-XOR).

4) Activity: We use activity as a technology-agnostic way to compute the structural dynamic power drain of our proposed circuits. Due to the lack of an industrial production process, this is the closest that we can get toward energy estimates for emerging technology circuits. We calculate activity for each logic gate by determining the two input patterns, differing in exactly one bit, which affect the most transistors along all possible paths to all affected outputs. That is the maximum number of transistors that is affected by the transition from the first to the second input pattern. As we compute the critical delay for a circuit under the assumption that only one input bit is changing, in the same way here, we do not consider multiple simultaneous changes of the circuit inputs for our activity calculations.

In Fig. 5, we show the activity of the multifunctional circuit as an example. There are various possible input combinations, over the four inputs A, B, S1, and S2, that excite the logic gates in various ways. For example, if input A would have been changed, keeping all other inputs fixed, then, three transistors in 3-MIN and four in 3-XOR would be affected. The same would be true for the input B. However, a change in input S1 (shown in red) affects the maximum number of transistors in the first stage—five for in 3-MIN and six for in 3-XOR (shown as red numbers). Similarly, for the multiplexer and the buffer, the maximum number of transistors are affected when S2 would change, i.e., six and four, respectively, for each logic gate. But as our initial assumption was that only single bit input changes are allowed, so we keep changing S1 only. Thus, the multiplexer is affected by its selected inputs, reducing its activity from 6 to 2. Hence, the total activity for the circuit comes out to be $5 + 6 + 2 + 4 = 17$.

Our activity calculations in Table III show that the structural benefits of runtime reconfiguration not only reflect in the area and delay but also in the circuit's activity. It can be noticed that for the runtime-reconfigurable circuit, the activity is the least, as it has the smaller logic gates and hence the number of transistors is also less. So, the runtime reconfigurable implementations not only perform a given function faster but also with less activity per operation.

V. Case Study: 1-bit ALU Circuit

The multifunctional circuit shown in the previous section clearly gives an insight into how a wide range of logic functions can be derived from circuits made using reconfigurable FETs. In this section, we demonstrate how an important circuit such as an ALU can be made more efficiently with RFETs.

In the previous section, the RFET MUX-tree circuit is the largest (by 31%) of the lot as compared with the CMOS circuit. In a simple one-to-one comparison, CMOS circuits will often gain as compared with the RFET circuits because of the smaller size of the individual transistor. Hence, tailored approaches to circuit design are highly imperative for newer nanotechnology such as RFETs. Such circuit designs should precisely and efficiently employ the feature set of these new devices.

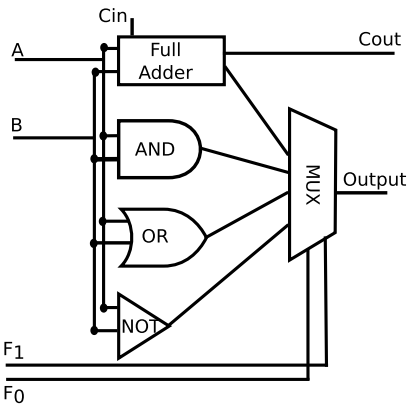

Fig. 6. Gate-level representation of generic 1-bit ALU based on CMOS.

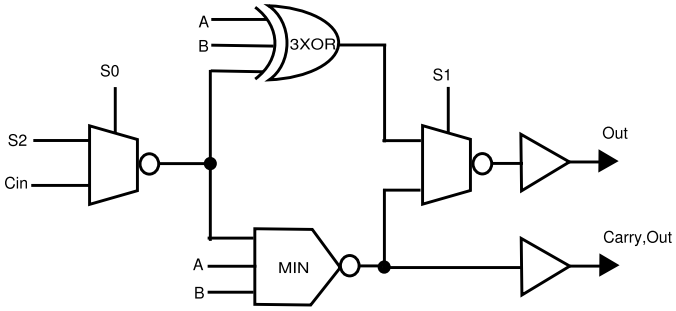

Fig. 7. Novel gate-level representation of generic 1-bit ALU based on RFETs.

TABLE V
Novel ALU Selection Signals

S0	S1	S2	Out
0	0	0	NOR
0	0	1	NAND
0	1	0	XOR
0	1	1	XNOR
1	0	n/a	MAJ
1	0	n/a	MAJ
1	1	n/a	FA
1	1	n/a	FA

Rai *et al.* [46] showed that an ALU is also an example circuit, which uses runtime reconfigurability. The reconfigurable nature of an ALU is possible due to the presence of 4-to-1 MUX which selects a specific functional output depending on the assignment of the select lines. In this case, the circuit basically computes all the functional outputs, such as AND, OR, XOR, and full adder. This is shown in Fig. 6. It is to be noted that the ALU used here is a representative figure containing major components.

We propose here an innovative design of the representative 1-bit ALU using reconfigurable FET-based logic gates as shown in Fig. 7. In Section V-A, we detail the design features of this ALU circuit based on reconfigurable transistors. We support our design with a comparative study with the CMOS-based circuit in terms of delay, area, and power, respectively.

TABLE VI
COMPARISON IN TERMS OF AREA, NORMALIZED DELAY, AND ACTIVITY FOR THE 1-bit ALU DESIGNS SHOWN IN FIGS. 6 AND 7

Circuit	Area (μm^2)	% area gain w.r.t. CMOS	Total Normalized Delay	% delay gain w.r.t. CMOS	Activity	% activity gain w.r.t. CMOS
ALU reconf (Fig. 7)	3.88	30.02	23.9	34.47	23	36.11
ALU_RFETs (Fig. 6)	9.50	-71.48	20.18	44.67	36	0
ALU_CMOS (Fig. 6)	5.54	Reference	36.47	Reference	36	Reference

A. Novel Design of 1-bit ALU

We propose the circuit for a 1-bit ALU as shown in Fig. 7. The starting point for our novel design was the CMOS circuit (see Fig. 6). Intuitively, one can see that the AND, OR, and NOT logic gates can be replaced by a single MIN gate (an additional inverter for AND and OR operation). With that approach, we replace the AND-OR functionality of the ALU with a majoriy (MAJ) logic gate. This is implemented using a 3-RFET MIN logic gate and an inverter. Hence, with a single MIN logic gate, one can generate all of the above functionality. For the full adder implementation, we stripped the full adder circuit in the normal ALU circuit and used only a 3-bit XOR instead. The 3-bit XOR will assume functionality in case of the pass transistor logic. Hence, the basic set of logic functions offered by the circuit of Fig. 4 is taken by these two logic gates. We refer to this circuit as the ALU_reconf in our calculations.

After this, a MUX is used to carefully connect the above two logic gates to select the required functionality. By intelligent use of S0 and S2, one can toggle among various logic functionalities. The selection of S0, S1, and S2 to achieve different functionalities is shown in Table V. The MUX with select lines S1 selects the output from the inputs from either the MIN or the 3-bit XOR.

The first MUX selects the AND/OR functionality from the MIN gate to calculate C_{out}. The value of the select signal S0 needs to be 1 to select the C_{in} and to calculate the C_{out}. In other cases, where S0 is 0, S2 is passed, which enables the circuit to have either the AND gate or the OR gate. For C_{out} calculation, the MAJ logic function is used and C_{in} is the third input as evident from Table V.

The truth table as shown in Table V also shows that this novel ALU can deliver other additional logic functions as well. The novel ALU design based on reconfigurable FETs is capable of producing more functions, which is just a bonus as compared with the contemporary technologies. For example, XNOR, which is one of the most important functionality for equality comparison, can easily be achieved just by configuring the 3-bit XOR logic gate.

B. Results and Discussion

Table VI shows the area, delay, and activity calculation for the existing and the novel 1-bit ALU circuit. Furthermore, we have considered the original CMOS-based ALU design in terms of RFET (termed ALU_RFET in Table VI) and included parameters for this version of circuit as well. The CMOS circuit is our baseline reference for all the calculations.

For area calculation, the area is calculated as mentioned in the previous section. The area for novel ALU (ALU_reconf) comes out to be 30% smaller as compared with the CMOS counterpart. If the generic ALU shown in Fig. 6 is built from RFET, the area is 70% larger than that of the CMOS counterpart. That is coherent in terms of the sizes of individual transistors in RFET and CMOS technologies and also backs our starting claims.

In terms of delay, as calculated using the logic effort theory (as mentioned in the previous section), it is to be noted that the RFET-based circuits have higher performance as compared with the CMOS circuit primarily because of the reduced critical path of the overall circuit which can be attributed to the transistor-level reconfigurability. The ALU_RFETs is faster than the ALU_reconf as the latter uses the pass transistor logic. The pass transistor logic is slower in performance but gains in higher functional expression. The RFET-based circuits are 44% and 34%, respectively, faster than the CMOS-based circuit.

It has to be taken into account that MIGRFETs comprise the combination of fast inputs (low $|Vt|$) and a slow input (high $|Vt|$) (compare with the characteristics given in Fig. 1 as CG terminal's I–V characteristics have a steeper slope [34]). Hence, care has to be taken in the circuit design that the output from the first MUX is not connected to the input in the pass transistor logic as that will add to the circuit delay. Hence, a clever optimization is to apply this input to one of the middle CG inputs of the transistor. In this case, one of the signals, A or B, has to be connected in the pass transistor logic.

For power calculations, we have used the same activity metric as in the previous section. The activity is the least in the reconfigurable mode. Activity is an indicative metric to extrapolate the power dissipation of circuits based on RFET nanotechnology.

The circuit shown in Fig. 7 gives a strong statement for the number of functions that can be achieved by using RFETs. Furthermore, the functional range is higher as compared with the traditional ALU. Intelligent design approaches have to be taken in case of circuits made of novel emerging nanotechnologies in order to truly harness their benefits.

VI. CONCLUSION

In this paper, we have presented the new compact and efficient designs of combinational logic gates. These are enabled by reconfigurable nanowire transistors with multiple independent gates, which can be used to replace arrangements of multiple transistors in series. This leads to several differences in circuit topology, e.g., NAND, NOR, and MUX all provide

inverter drive capability. We found that the logic gates based on reconfigurable transistors are functionally enhanced. We have shown the example of multifunctional and dynamically programmable circuit with reduced normalized delay and an estimated postsynthesis area numbers. The equivalent functional circuit based on SiNW technology occupies 20% (pass transistor mode) less area as compared with the CMOS reference circuit. In terms of normalized circuit delay as estimated by logical effort calculations as a technology-agnostic measure, the RFET-based implementations are 32% faster than the CMOS reference circuit, under the assumption that a similar performance of the individual devices can be achieved. Note that the disruptive reconfigurable technology is not limited to silicon and is expandable to other semiconductor materials, such as germanium [18] and carbon [4], [29]. The exquisite feature lies in the ease of extended functionality which the RFET nanotechnology can provide.

Furthermore, we presented a novel design for a 1-bit ALU circuit based on RFET technology in which the gains in terms of area is 30%, in terms of circuit delay is 34%, and in terms of activity is 36% as compared with the CMOS technology. We have shown how efficient circuit design using reconfigurable transistors can lead to a range of benefits over contemporary CMOS technologies. The technology, albeit in its infancy, has shown a lot of promise in showing better numbers for area and delay. Various other works [31], [52], [53] have shown the efficacy of this technology in terms of area, power, and delay, respectively, catering to the static logic. Newer technology solutions delivering a more compact structure of RFETs, such as vertical technologies, can play a major role in further reducing area for circuits based on RFETs. Newer approaches have to be developed at the logic and physical synthesis-level for gaining optimum performance from novel nanotechnologies.

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